FORM PTO-1449	ATTY. DOCKET NO. 200304950-2	APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets If necessary)	APPLICANT David Arthur James Webb, Jr. et al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
CH	1A	5,872,946	02/16/99	Narayan et al.	
CH	1B	5,155,843	10/13/92	Stamm et al.	
CH	1C	4,847,755	07/11/89	Morrison et al.	
CH	1D	4,229,790	10/21/80	Gilliland et al.	
CH	1E	6,542,987 B1	04/01/03	Fischer et al.	
CH	1F	5,870,578	02/09/99	Mahalingaiah et al.	
CH	1G	6,115,807	09/05/00	Grochowski	
CH	1H	6,112,019	08/29/00	Chamdani et al.	
CH	1I	5,627,983	05/06/97	Popescu et al.	
CH	1J	5,822,559	10/13/98	Narayan et al.	
CH	1K	6,182,210 B1	01/30/01	Akkary et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check If Translation attached
	1L					
	1M					
	1N					
	1O					
	1P					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

CH	1Q	Keller, J., "The 21264: A Superscalar Alpha Processor with Out-of-Order Execution," Paper present at the Microprocessor Forum on October 22-23, 1996
C H	1R	Gieseke, Bruce A. et al., Digital Semiconductor, Digital Equipment Corporation, "A 600MHz Superscalar RISC Microprocessor with Out-Of-Order Execution," ISSCC97/Session 10/High-Performance Microprocessors/Paper FA 10.7, IEEE International Solid-State Circuits Conference, 176-177, 451, (1997).
C H	1S	Farrell, J.A. and Fischer, T.C., "Issue Logic for a 600-MHz Out-of-Order Execution Microprocessor," J. Solid-State Circuts 33(5):707-712 (1998).

EXAMINER	DATE CONSIDERED 3/3/05

Rev 10/03 (PTO1449)

FORM PTO-1449	ATTY. DOCKET NO. 200304950-2	APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	APPLICANT David Arthur James Webb, Jr. et al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
C H	2A	6,148,394	11/14/00	Tung et al.	
	2B				
	2C				
	2D				
	2E				
	2F				
	2G				
	2H				
	2I				
	2J				
	2K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	2L					
	2M					
	2N					
	2O					
	2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

C H	2Q	Scott, A.P., et al., "Four-Way Superscalar PA-RISC Processors," J. Hewlett-Packard 1:1-9 (August 1997).
C H	2R	Farrell, J.A. and Fischer, T.C., "Issue Logic for a 600-MHz Out-of-Order Execution Microprocessor," J. Solid-State Circuts 33(5):707-712 (1998).
C H	2S	Gwennap, Linley, "Digital 21264 Sets New Standard," Microdesign Resources, Microdesign Report (October 28, 1996).

EXAMINER	DATE CONSIDERED
	3/3/05

Rev 10/03 (PTO1449)

FORM PTO-1449 LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)	ATTY. DOCKET NO. 200304950-2	APPLICATION NO.	CONFIRMATION NO.
	APPLICANT David Arthur James Webb, Jr. et al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	3A				
	3B				
	3C				
	3D				
	3E				
	3F				
	3G				
	3H				
	3I				
	3J				
	3K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	3L					
	3M					
	3N					
	3O					
	3P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

CH	3Q	A Tour of the P6 Microarchitecture [online], [retrieved on 1999-03-10]. Retrieved from the Internet < URL:http://eecad.sogang.ac.kr/AboutSite+ Others/Others/intel/procs/p6/p6white/p6white.htm> .
CH	3R	A 56-Entry Instruction Reorder Buffer [online], [retriened on 1999-03-10]. Retrieved from the Internet URL:http://www.hp.com/ahp/framed/technology/micropro/micropro/pa-8000/docs/56entry.html> .
CH	3S	Fischer, T. and Leibholz, D., "Design Tradeoffs in Stall-Control Circuits for 600MHz Instruction Queues," Paper presented at the IEEE International Solid-State Circuits Conference (February 1998).

EXAMINER	DATE CONSIDERED
[signature]	3/3/05

FORM PTO-1449	ATTY. DOCKET NO. 200304950-2	APPLICATION NO.	CONFIRMATION NO.
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if n cessary)	APPLICANT David Arthur James Webb, Jr. et al.		
	FILING DATE	GROUP	

REFERENCE DESIGNATION   U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
	4A				
	4B				
	4C				
	4D				
	4E				
	4F				
	4G				
	4H				
	4I				
	4J				
	4K				

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
	4L					
	4M					
	4N					
	4O					
	4P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

C H	4Q	Kessler, R.E., Compaq Computer Corporation, "The Alpha 21264 Microprocessor," IEEE Micro 24-36 (March-April 1999).
C H	4R	Liebholz, Daniel and Razdan, Rahul, Digital Equipment Corporation, "The Alpha 21264: A 500 MHZ Out-of-Order Execution Microprocessor," from Compcon February, 1997 Proceedings.
C H	4S	Popescu, V. et al., "The Metaflow Architecture," IEEE Micro, Vol. 11, Issue 3, June 1991, pp. 10-13, 63-73.

EXAMINER	DATE CONSIDERED
	3/21/05

Rev 10/03 (PTO1449)